

Short Paper

NUMERICAL EVALUATION OF THERMAL CYCLING RELIABILITY OF HIGH PERFORMANCE FLIP-CHIP PACKAGE ASSEMBLY USING SUBMODELING ANALYSIS

Chin-Li Kao, Yi-Shao Lai*, and Tong Hong Wang

ABSTRACT

This paper applies the submodeling technique in analyzing thermal cycling reliability of high performance flip-chip ball grid array package assemblies. The packages have one-piece tunnel-type heat spreaders with different lead widths, connected to chips using different thermal interface materials. The global model contains no solder bumps to simplify the analysis. The calculated displacement field of the global model is then interpolated on the boundary of the submodel that contains the critical solder bump. The submodel is solved using the prescribed displacement boundary conditions together with external thermal loads to evaluate thermomechanical reliability of the critical solder bump.

Key Words: submodeling, finite element analysis, thermal cycling, high-performance flip-chip package.

I. INTRODUCTION

The trend of contemporary electronic packaging is toward miniaturization and high I/O density. Unlike the conventional wirebond technology that passes electric signals through bonded wires, for which I/O is only allowed to take place on the periphery of the chip, the flip-chip technology makes use of solder bumps as interconnects and hence enables the entire surface of the chip to be fully utilized. Moreover, the absence of bonded wires also reduces signal inductance.

The tremendous number and delicate structures of solder bumps bring arduous modeling tasks to the analysts who are involved in the numerical analysis of flip-chip packages. With limited computational resources, performing of a full-scale three-dimensional thermomechanical analysis is impossible

without simplifying the solder interconnects to a certain extent. Methodologies have been proposed to simplify the modeling of solder interconnects so that the computational complexity can be reduced to a reasonable scale (Corbin, 1994; Gu *et al.*, 2001; Chan *et al.*, 2002; Vandeveld *et al.*, 2003; Yuan and Chiang, 2003; Kao *et al.*, 2003; Wang and Lai, 2005; Lai and Wang, 2005). Among them, the submodeling technique (Gu *et al.*, 2001; Chan *et al.*, 2002; Yuan and Chiang, 2003; Wang and Lai, 2005; Lai and Wang, 2005) is particularly feasible in analyzing localized behavior of a large model.

Since, in practical use, the solder interconnects are subjected to high homologous temperatures, temperature-dependent plasticity is supposed to dominate their deformation kinetics (Skrzypek, 1993). Careful numerical treatments are therefore required for submodeling analyses for problems which involve path-dependent characteristics or otherwise the solution would be improper or incorrect. To cope with the problem, Wang and Lai (2005) managed to propose a way of properly solving path-dependent thermomechanical problems using the submodeling

*Corresponding author. (Tel: 886-7-3617131 ext. 85285/15285; Fax: 886-7-3613094; Email: yishao_lai@aseglobal.com)

The authors are with the Stress-Reliability Lab, Advanced Semiconductor Engineering, Inc., Nantze, Kaohsiung 811, Taiwan.

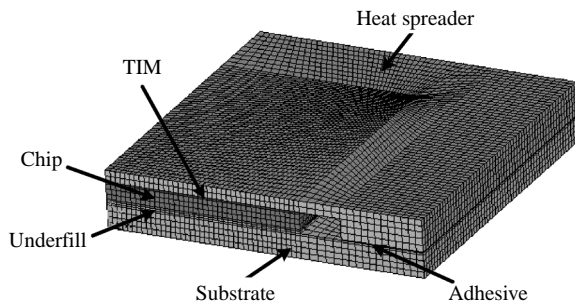


Fig. 1 Quarter symmetry global model

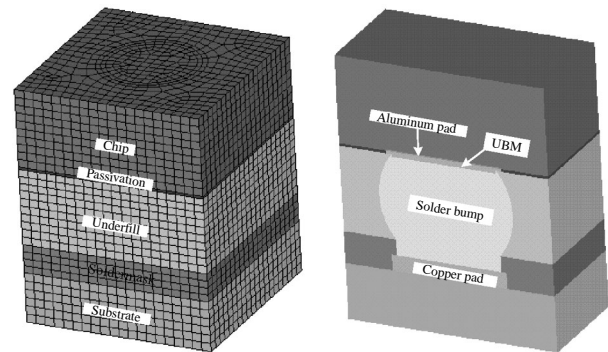


Fig. 2 Submodel and cross-section

technique without *a priori* assumptions.

In this paper we apply the submodeling procedure proposed by Wang and Lai (2005) to analyze the thermal cycling reliability of a high performance flip-chip ball grid array (HFCBGA) package assembly. The package has a one-piece tunnel-type heat spreader attached using thermal interface material (TIM) to enhance its thermal dissipation capability in order to comply with the demands of high power. The paper is dedicated to demonstrating the application of the submodeling technique in analyzing this particular HFCBGA package assembly that involves path-dependent thermomechanical characteristics.

II. FINITE ELEMENT MODELING

We consider two HFCBGA package assemblies whose dimensions are $27 \times 27 \times 2.4 \text{ mm}^3$ and $31 \times 31 \times 2.4 \text{ mm}^3$. The corresponding chip dimensions are $20.5 \times 16.5 \times 0.74 \text{ mm}^3$ and $18 \times 18 \times 0.74 \text{ mm}^3$, respectively. Each of the packages features a 1.36 mm thick one-piece tunnel-type direct-lead-attach (DLA) heat spreader attached to the 1 mm thick substrate through its leads. The lead width is 3.5 mm, 2.8 mm, 2.0 mm, or 0, for which the heat spreader is flat and does not feature leads. The heat spreader is connected to the chip using different thermal interface materials of 85 μm thickness, whose effects are also examined.

The quarter symmetry global model is shown in Fig. 1. To simplify the analysis, the global model involves no solder bumps and the substrate is treated as a homogeneous layer. For the submodeling analysis of a flip-chip package, solution discrepancies on the solder bump corresponding to different abridged global models were examined by Lai and Wang (2005) through two-dimensional analysis. It was figured out that since disturbances in the displacement field due to the presence of solder bumps are quite localized, the accuracy of the submodeling solution is still acceptable without the solder bumps implemented in the global model.

Figure 2 shows the submodel and its cross-section. The submodel involves detailed and delicate structural components of a single solder bump located at the outermost diagonal corner of the fully populated bump array, which is generally considered the most critical location of the entire bump array. The submodel is 255 μm thick, containing one-third of the chip and one-third of the substrate. Each of the lateral dimensions of the submodel is 200 μm , identical to the pitch between adjacent solder bumps. The solder bump is soldermask-defined, for which the soldermask is 30 μm thick and its opening is 100 μm . The diameter of the solder bump is 130 μm while the standoff is 85 μm after flip-chip bond. The diameter and thickness of the aluminum pad are 110 μm and 2 μm , respectively while those of the copper pad are 110 μm and 15 μm , respectively. The under bump metallurgy (UBM) is 3 μm thick and the passivation is 1.5 μm thick. To simplify the analysis, the UBM is modeled as a single piece of copper. The submodel contains 14,278 linear hexahedral elements and 48,000 degrees of freedom.

Since the mechanical response of the solder bump is of concern, boundaries of the submodel should be sufficiently far from the encompassed solder bump in order for the St. Venant's principle to be valid, which assures that the boundary effect will produce insignificant disturbances on local solutions. Though we do not intend to study the dimension effect in this paper, the verification work by Lai and Wang (2005) implies that the dimension we choose for the submodel may well suit the purpose.

Elastic properties of the constituent components are given in Table 1. The solder bump composition is eutectic 63Sn-37Pb. Parameters for the Anand viscoplastic constitutive model (e.g., Wilde *et al.*, 2000) for this specific solder alloy are $C_1 = 12.41 \text{ MPa}$, $C_2 = 9400 \text{ K}$, $C_3 = 4 \text{ Ms}^{-1}$, $C_4 = 1.5$, $C_5 = 0.303$, $C_6 = 1375.98 \text{ MPa}$, $C_7 = 13.79 \text{ MPa}$, $C_8 = 0.07$, and $C_9 = 1.30$ (Darveaux, 2002), arranged in the manner recognized by ANSYS.

Table 1 Elastic properties of constituent components

Component	Young's modulus (GPa)	Coefficient of thermal expansion (ppm/°C)	Glass transition temperature (°C)	Poisson's ratio
Chip	131	2.8	–	0.28
Passivation	2.9	52	–	0.34
Alumium	117.6	24	–	0.16
Copper	121	21.1	–	0.38
Soldermask	2.41	60/160	104	0.40
Substrate	19.8@-55°C 12.2@150°C	16	–	0.20
Adhesive	11.56@-50°C 0.04@150°C	58/178	42	0.35
Underfill	7@-55°C 0.04@200°C	32/110	70	0.30
63Sn-37Pb	42.78@-55°C 15.47@125°C	24.5	–	0.35
TIM A	0.007	110	–	0.35
TIM B	0.004	220	–	0.35

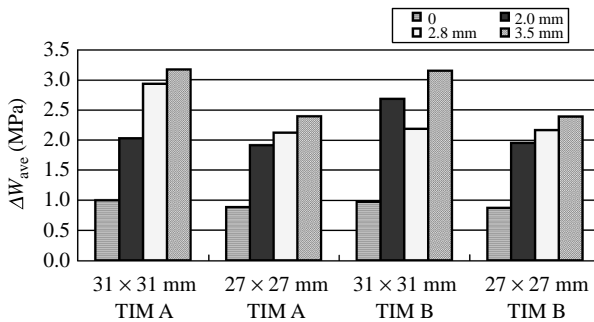


Fig. 3 The ΔW_{ave} on top region of bump

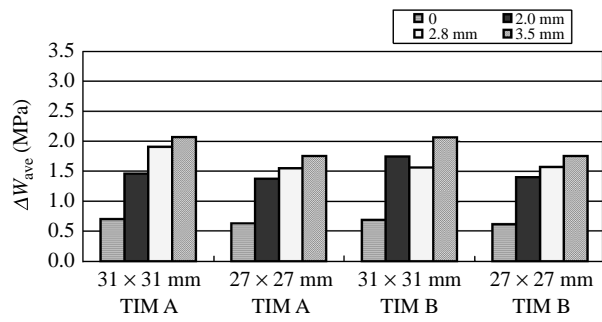


Fig. 4 The ΔW_{ave} on bottom region of bump

The analysis is carried out using ANSYS v. 7.0. Quadratic quadrilateral elements are utilized. The stress-free temperature is set at 150°C, the curing temperature of the underfill. The temperature cycled two times between -40°C and 125°C, following the sequence of 15-min ramping to cold, 15-min dwelling at cold, 15-min ramping to hot, and 15-min dwelling at hot.

III. THERMAL CYCLING RELIABILITY

Since the Anand viscoplastic constitutive model is applied in this paper, the evaluation of the fatigue life is based on the viscoplastic strain energy density accumulated per thermal cycle on the most critical solder bump, encompassed in the submodel. The

averaged viscoplastic strain energy densities accumulated per thermal cycle on the volumetric regions that cover 25.4 μm from the top and the bottom surfaces of this particular solder bump are utilized to evaluate the fatigue resistance of the solder bump. The volumetric averaging technique,

$$\Delta W_{ave} = \frac{\sum \Delta W \cdot V}{\sum V},$$

is applied to reduce solution sensitivity in regard to the mesh density. In the above equation, ΔW is the viscoplastic strain energy density accumulated per thermal cycle in an element within the evaluation region, and V is the volume of the corresponding element. The ΔW_{ave} on the top and bottom regions for HFCBGA with different structural settings are

shown in Fig. 3 and Fig. 4, respectively.

Comparing these two figures, we notice that thermal cycling fatigue fracturing may occur around the top region of the most critical solder bump. The heat spreader without leads leads to the longest fatigue life among different heat spreader designs. Moreover, the DLA heat spreader with a wider lead has a shorter fatigue life except for the 31 mm squared HFCEGA with TIM B, for which the heat spreader with a 2.0 mm wide lead results in a shorter fatigue life than that with a 2.8 mm wide lead. Apart from these two particular cases, the adoption of TIM A or TIM B does not affect significantly the fatigue reliability of solder bumps. The considerable effect of TIM materials on the fatigue reliability of solder bumps for the two particular cases may possibly be a result of the specific packaging structural configurations, which indeed requires further examination.

We would also like to point out that in this study, the interfaces between the thermal interface material and the chip as well as the heat spreader are assumed perfectly bonded without sliding. In reality, however, certain thermal interface materials do not provide tight adhesions to the chip or to the heat spreader. To deal with these particular materials, an advanced numerical treatment incorporating sliding contact is needed.

IV. CONCLUSIONS

This paper demonstrates the use of the submodeling technique in the analysis of path-dependent thermomechanical problems through examining thermal cycling reliabilities of high performance flip-chip packages equipped with tunnel-type DLA heat spreaders of different lead widths, connected to the chip using different thermal interface materials. From the analysis we notice that for most of the packaging structural configurations proposed in this study, the adoption of different thermal interface materials does not affect significantly the fatigue reliability of the solder bumps.

The submodeling technique demonstrated in this paper presents a methodology conducive to the analysis of the thermomechanical fatigue reliability of solder interconnects, which are in general great in number and delicate in structure and therefore extremely difficult to be dealt with owing to limited computational resources.

REFERENCE

- Chan, Y. W., Ju, T. H., Hareb, S. A., and Lee, Y. C., 2002, "Reliability Modeling for Ball Grid Array Assembly with a Large Number of Warpage Affected Solder Joints," *Journal of Electronic Packaging*, ASME, Vol. 124, No. 3, pp. 246-253.
- Corbin, J. S., 1994, "Finite Element Analysis of Solder Ball Connect (SBC) Structural Design Optimization," *IBM Journal of Research and Development*, Vol. 37, No. 5, pp. 585-596.
- Darveaux, R., 2002, "Effect of Simulation Methodology on Solder Joint Crack Growth Correlation and Fatigue Life Prediction," *Journal of Electronic Packaging*, ASME, Vol. 124, No. 3, pp. 147-154.
- Gu, Y., Nakamura, T., Chen, W. T., and Cotterell, B., 2001, "Interfacial Delamination Near Solder Bumps and UBM in Flip-Chip Packages," *Journal of Electronic Packaging*, ASME, Vol. 123, No. 3, pp. 295-301.
- Kao, C.-L., Lai, Y.-S., and Wu, J.-D., 2003, "Application of Incompatible Mesh in Three-Dimensional Analysis of Flip-Chip Ball Grid Array Assembly," *Proceedings of the IMAPS Taiwan Technical Symposium 2003*, Kaohsiung, Taiwan, pp. 230-235.
- Lai, Y.-S., and Wang, T. H., 2005, "Verification of Submodeling Technique in Thermomechanical Reliability Assessment of Flip-Chip Package Assembly," *Microelectronics Reliability*, Vol. 45, No. 3-4, pp. 575-582.
- Skrzypek, J. J., 1993, *Plasticity and Creep*, CRC Press, Boca Raton, USA.
- Vandeveld, B., Degryse, D., Beyne, E., Roose, E., Corlatan, D., Swaelen, G., Willems, G., Christiaens, F., Bell, A., Vandepitte, D., and Baelmans, M., 2003, "Modified Micro-Macro Thermo-Mechanical Modelling of Ceramic Ball Grid Array Packages," *Microelectronics Reliability*, Vol. 43, No. 2, pp. 307-318.
- Wang, T. H., and Lai, Y.-S., 2005, "Submodeling Analysis for Path-Dependent Thermomechanical Problems," *Journal of Electronic Packaging*, ASME, Vol. 127, No. 2, pp. 135-140.
- Wilde, J., Becker, K., Thoben, M., Blum, W., Jupitz, T., Wang, G., and Cheng, Z. N., 2000, "Rate Dependent Constitutive Relations Based on Anand Model for 92.5Pb5Sn2.5Ag Solder," *IEEE Transactions on Advanced Packaging*, Vol. 23, No. 3, pp. 408-414.
- Yuan, C.-A., and Chiang, K.-N., 2003, "Micro to Macro Thermo-Mechanical Simulation of Wafer Level Packaging," *Journal of Electronic Packaging*, ASME, Vol. 125, No. 4, pp. 576-581.

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